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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/124,649	07/29/98	NGAI	T ALT-155

EXAMINER

BATAILLE,P

ART UNIT	PAPER NUMBER
2186	17

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TM21/0706

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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/124,649	Ngai et al.
Examiner	**Group Art Unit**
P. Batalle	2186

☒ Responsive to communication(s) filed on *May 10, 2001*

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire *3* month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) *1-12* is/are pending in the applicat

Of the above, claim(s) _____ is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-12* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment filed May 10, 2001 in response to PTO Office Advisory Action dated May 2, 2001. The applicant's remarks and amendment the claims were considered with the results that follow.

2. Claims 1-12 were previously presented for examination in this application. Of the previously presented claims, claims 1, 3-4, 7, and 9-10 have been amended to more clearly present the claimed invention. No claims have been canceled or added. Therefore, all claims 1-12 remain pending in the application.

Response to Arguments

3. Applicant's arguments filed October 26, 2000, with respects to claims 1-12, have been fully considered but they are moot in view of new grounds of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heile (US6,020,759) in view of Young (US5,933,023).

As per claims 1-2 and 7-8, Heile teaches a programmable logic array device [Fig. 2] comprising: a plurality of logic resources [logic blocks 21, Fig. 2]; a plurality of group of interconnection conductors for interconnecting said logic resources [interconnection conductor network 23, Fig. 2]; and a plurality of programmable interconnection resources for connecting conductors in said group of said interconnection conductors and to said plurality of logic resources [13, 18, 19, 103 & 107, Fig. 1], said programmable interconnection resources being less than fully populated [Col. 5, Lines 18-31, Lines 42-51]; said programmable logic array device includes

at least one random access memory device [10, Fig. 1 & 2] (Col. 3, Lines 7-10) having a read port [dataout conductor 110, Fig.1] and a write port [datain bus conductors 12, Fig. 1] (Col. 3, Lines 11-14); a first programmable interconnection resource [103, Fig. 1] in said plurality of interconnection resources for connecting port conductors in said read port to a selected one of said plurality of group of interconnection conductors [Col. 3, Lines 39-55]; and a second programmable interconnection resource [13, Fig. 1] in said plurality of interconnection resources for connecting port conductors in said write port to a selected one of said plurality of group of interconnection conductors [Col. 3, Lines 15-31]; wherein said first and second programmable interconnection resources are populated to allow connection of an individual conductor in said

selected one of said plurality of groups of interconnection conductors to corresponding port conductors in said read port and said write port [Fig. 4 & 5; Col. 3, Line 50 to Col. 4, Line 12].

As per claims 3-6 and 9-12, Heile teaches the programmable logic device shown in a data processing system [502, Fig. 7] including components such as a processor 504, memory board 506 and I/O circuitry 508 and other peripheral devices [Col. 6, Lines 30-33], and the said components mounted on a printed circuit board 530 [Col. 6, Lines 33-37].

Independent claims 1, 3-4, 7, and 8-9 require that the interconnection resources are less than fully populated and RAM memory having a read port having a number of read port conductor and a write port having a second number of write port conductors equal to the number of read port conductors. However, the applicant admits that "it is well known in programmable logic devices, a less than fully populated interconnection resource allows each conductor to in one group of conductors to access at least one conductor in another group". Moreover, Young teaches programmable logic devices or field programmable gate arrays formed in integrated circuits comprising an array of programmable logic blocks which can be programmably interconnected to each other employing dual ported RAMs [Fig. 2], each RAM is a dual port RAM and can be configured as two separate single-port RAMs, or as one single-port RAM [Col. 9, Lines 56-59], the RAM memory having a read port having a number of read port conductor and a write port having a second number of write port conductors equal to the number of read port conductors [Fig. 2, Fig. 7A; Col. 4, Lines 49-66] wherein local interconnect lines make

programmable connections [Fig. 4] which can be in turn programmably connected to local clock line LCLK1 and in turn be connected to clock input terminal CKB or CKA of either the B or the A port, i.e. each interconnection resource is allowed selective connection to each individual conductor in a selected way to an individual read port conductor and to an individual write port conductor [Col. 6, Lines 2-41; Col. 7, Lines 5-35; Col. 9, Lines 13-49].

Therefore it would have been obvious that the feature recited the programmable interconnection resources would not be patentable as it is common in programmable logic devices, admitted by the applicant [applicant's communication on page 13] and it would have been obvious to one having ordinary skill in the art and having the teaching of Heile and Young before him at the time of the invention to combine the two teachings since, as taught by Young, fewer programmable interconnection point (PIP) would minimize chip area provide the greatest flexibility and speed for common uses of the structure and sufficient number of local interconnect lines would be sufficient for a user to access all address, data, and control lines used in a configuration [Col. 6, Lines 52-64].

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 6,191,998 Reddy et al. Feb. 20, 2001

Contact Information

7. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 305-9731 (for informal or draft communications,

please label "PROPOSED" or "DRAFT");

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre-Michel Bataille whose telephone number is (703) 301-0134. The examiner can normally be reached on Tuesday to Friday from 7:30 A.M. to 6:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew M. Kim, can be reached on (703) 305-3821. The fax phone number for this Group is (703) 305-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

PB.

P. Bataille

July 5, 2001

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100